Listing of the Claims

1. (Original) A method for forming a single transistor planar RAM memory cell with improved charge retention comprising the steps of:

providing a silicon substrate comprising an STI structure and an overlying dielectric gate layer;

depositing a polysilicon layer;

forming a pass transistor structure adjacent a storage capacitor structure separated by a predetermined distance;

carrying out a first ion implantation process to form first and second doped regions adjacent either side of the pass transistor structure, the first doped region defined by the predetermined distance;

depositing a spacer dielectric layer;

etching back the spacer dielectric layer to leave an unetched spacer dielectric layer portion overlying the first doped region while forming a sidewall spacer of a predetermined width overlying a first portion of the second doped region; and,

carrying out a second ion implantation process to form a relatively higher dopant concentration in a second portion of the second doped region.

2. (Original) The method of claim 1, further comprising the step of forming self aligned silicide regions over the second portion, the pass transistor structure and the storage capacitor structure.

3. (Original) The method of claim 1, wherein the dielectric gate layer is selected from the group consisting of SiO_2, nitrided SiO_2, and oxide/nitride.

4. (Original) The method of claim 1, wherein the dielectric gate layer comprises material selected from the group consisting of Ta_2O_5, TiO_2, HfO_2, Y_2O_3, La_2O_5, ZrO_2, BST, and PZT.

5. (Original) The method of claim 1, wherein the storage capacitor structure is formed at least partially overlying the STI structure.

6. (Original) The method of claim 1, wherein the predetermined distance is less than about twice the predetermined width.

7. (Original) The method of claim 1, wherein the spacer dielectric layer thickness is about greater than about half of the predetermined distance.

8. (Original) The method of claim 1, wherein the pass transistor structure and the storage capacitor structure comprise a memory cell formed over an N doped well region of a P doped silicon substrate.

9. (Original) The method of claim 1, wherein the first and second doped regions respectively comprise P- and P+ doped regions.

10. (Original) The method of claim 1, wherein the first doped region is doped to a level of between about 10^{12} and 10^{14} dopant atoms/cm^2 and the second doped region comprises a relatively higher doped region of greater than about 10^{15} dopant atoms/cm^2.

11. (Original) The method of claim 1, wherein the spacer dielectric layer comprises one or more layers selected from the group consisting of silicon oxide, silicon nitride, and silicon oxynitride.

12. (Original) A method for forming a single transistor planar RAM memory cell with improved charge retention comprising the steps of:

providing a silicon substrate comprising an STI structure and an overlying dielectric gate layer;

depositing a polysilicon layer;

forming a pass transistor structure adjacent a storage capacitor structure separated by a predetermined distance for forming a first doped region;

carrying out a first ion implantation process to form the first doped region and a second doped region adjacent the pass transistor structure;

blanket depositing a spacer dielectric layer having a thickness about greater than the predetermined distance;

etching back the spacer dielectric layer to leave an unetched spacer dielectric layer portion overlying the first doped region while forming a sidewall spacer overlying a first portion of the second doped region; and,

carrying out a second ion implantation process to form a relatively higher dopant concentration in a second portion of the second doped region.

13. (Original) The method of claim 12, further comprising the step of forming salicide regions over the second portion, the pass transistor structure and the storage capacitor structure.

14. (Original) The method of claim 12, wherein the dielectric gate layer is selected from the group consisting of SiO_2, nitrided SiO_2, and oxide/nitride.

15. (Original) The method of claim 12, wherein the dielectric gate layer comprises material selected from the group consisting of Ta_2O_5, TiO_2, HfO_2, Y_2O_3, La_2O_5, ZrO_2, BST, and PZT.

16. (Original) The method of claim 12, wherein the storage capacitor structure is formed at least partially overlying the STI structure.

17. (Original) The method of claim 12, wherein the predetermined distance is less than about twice the sidewall spacer width.

18. (Original) The method of claim 12, wherein the pass transistor structure and the storage capacitor structure comprise a memory cell formed over an N doped well region of a P doped silicon substrate.

19. (Original) The method of claim 12, wherein the first and second doped regions respectively comprise P- and P+ doped regions.

20. (Original) The method of claim 12, wherein the first doped region is doped to a level of between about 10^{12} and 10^{14} dopant atoms/cm^2 and the second doped region comprises a relatively higher doped region of greater than about 10^{15} dopant atoms/cm^2.

21. (Original) The method of claim 12, wherein the spacer dielectric layer comprises one or more layers selected from the group consisting of silicon oxide, silicon nitride, and silicon oxynitride.

22. (Withdrawn) A single transistor planar RAM device comprising:

a pass transistor structure and a storage capacitor structure formed over a silicon substrate and disposed is spaced apart relationship to form a spaced distance overlying a first doped region;

wherein sidewall spacer material is disposed adjacent either side of the pass transistor structure partially covering a second doped region and fully covering the first doped region.

23. (Withdrawn) The single transistor planar RAM device of claim 23, wherein the first doped region comprises a lower dopant concentration compared to the second doped region.

24. (Withdrawn) The single transistor planar RAM device of claim 24, wherein the first doped region is doped to a level of between about 10^{12} and 10^{14} dopant atoms/cm^2 and the second doped region comprises a relatively higher doped region of greater than about 10^{15} dopant atoms/cm^2.

25. (Withdrawn) The single transistor planar RAM device of claim 23, wherein the storage capacitor structure is disposed at least partially overlying a shallow trench isolation structure.

26. (Withdrawn) The single transistor planar RAM device of claim 23, further comprising salicide portions formed over a portion of the second doped region, the pass transistor structure, and the storage capacitor structure.

27. (Withdrawn) The single transistor planar RAM device of claim 23, wherein the pass transistor structure and the storage capacitor structure comprise a dielectric gate layer selected from the group consisting of SiO_2, nitrided SiO_2, and oxide/nitride.

28. (Withdrawn) The single transistor planar RAM device of claim 23, wherein the pass transistor structure and the storage capacitor structure comprise a dielectric gate layer comprising material selected from the group consisting of Ta_2O_5, TiO_2, HfO_2, Y_2O_3, La_2O_5, ZrO_2, BST, and PZT.

29. (Withdrawn) The single transistor planar RAM device of claim 23, wherein the pass transistor structure and the storage capacitor structure comprise a memory cell formed over an N doped well region formed in a P doped silicon substrate.

30. (Withdrawn) The single transistor planar RAM device of claim 23, wherein the first and second doped regions respectively comprise P- and P+ doped regions.

31. (Withdrawn) The single transistor planar RAM device of claim 23, wherein the pass transistor structure and the storage capacitor structure comprise P doped polysilicon electrode portions.

32. (Withdrawn) The single transistor planar RAM device of claim 23, wherein the spacer dielectric material comprises one or more layers selected from the group consisting of silicon oxide, silicon nitride, and silicon oxynitride.